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Review of VLSI Architecture of Cryptography Algorithm for IOT Security

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ABSTRACT: Privacy is key parameter of communication between or with internet of things. However, some of the challenges arising from the use of this algorithm are computational overhead, use of a fixed S-Box and pattern problems, which occur when handling more complex multimedia data such as text, image and video. Internet of things is promising to change the world to a better one with its tremendous applications in our daily lives where all physical objects will be connected to each other including humans. One major category of Internet of Things applications falls in the different industry like health, smart cities, Manufacture industries etc. Privacy is key parameter of communication between or with internet of things. Many researchers have carried out research aiming at improving the algorithm's performance. This paper summarizes the various research work based on encryption security algorithms and observed some constraint using in internet of things application.

KEYWORDS: Encryption, Security, Internet of Things (IoT), Privacy.

I. INTRODUCTION

The development of IoT by utilizing the new form of IP address (IPv6), which goes past the constraints of IPv4, will change the universe of Web by giving the network to a tremendous number of keen associated gadgets close to 70 billion, or considerably more. Prospering this innovation has been called as the Second Economy or the Modern Web revolution. It will create an enormous market with different administrations, and the extent of this market is assessed in the trillions of dollars. This market is a promising plan to be effective, anyway just if the security viewpoints get into record before this tremendous procedure begins to be actualized generally.

The IoT's anyplace, anything, whenever nature could undoubtedly change these points of interest into disservices, if security viewpoints would not be given enough. For instance, if anyone can approach any close to home administrations and data, or if the data of an extensive variety of individuals can be come to by nature consequently, the IoT would not have a dependable situation.

Multimedia data (text, audio, image, animation and video) have been widely used in the past few years for advanced digital content transmission. With the network technology focusing on Internet of Things (IoT) nowadays, the security of the multimedia content has raised researchers' concerns. The exchange of digital data over a network has exposed the multimedia data to various kinds of abuse such as Brute-Force attacks, unauthorized access, and network hacking. Therefore, the system must be safeguarded with an efficient media-aware security framework such as encryption methods that make use of standard symmetric encryption algorithms, which will be responsible for ensuring the security of the multimedia data.

For the encryption of electronic data, one of the most prominent cryptographic algorithms is the Advanced Encryption Standard algorithm. The Advanced Encryption Standard (AES) has been lately accepted as the symmetric cryptography standard for confidential data transmission. However, the natural and malicious injected faults reduce its reliability and may cause confidential information leakage. In this paper, we study concurrent fault detection schemes for reaching a reliable AES architecture. Specifically,

As networking technology advances, the gap between network bandwidth and network processing power widens. Information security issues add to the need for developing high-performance network processing hardware, particularly that for real-time processing of cryptographic algorithms.

Internet of Things security is the area worried about ensuring interconnected gadgets and systems in the biological community.

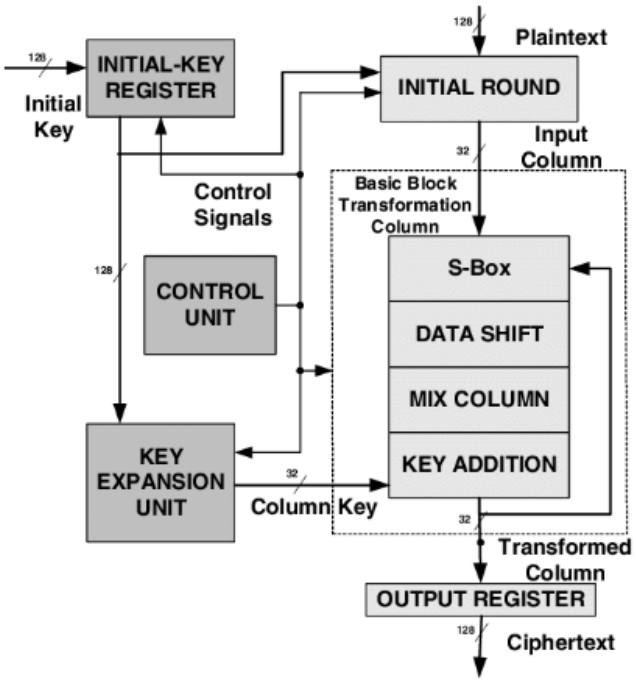

Figure 1: AES block diagram

In AES we have 128, 192 and 256 bit key size with 10, 12 and 14 rounds respectively. In AES the data and key is mixed to form key by implying, following steps.

a. Key Expansion:

Initially the key is expanded into two halves to form a bigger key using addition of padding bits.

b. Round Key:

Then we add round key (k1) with the initial key using XOR operation.

c. Round operation (N-1) rounds:

Usually we have 10, 12 and 14 rounds here, we usually follow the same steps for first(N-1) rounds and last Round will be different, here first we do substitution operation using look up table then rows are shifted, the Columns are mixed, each time round key is added to form new key.

d. Final Round:

In final round, when previous round key is added we do substitution, then shifting of rows and round key is added. Then finally all round keys are added to form a strong key.

II. BACKGROUND

T. B. Singha et. al., [1] The presented work carries out a Very Large Scale Integration (VLSI) implementation of the Advanced Encryption Standard (AES) symmetric cipher to investigate for its best-suited architecture for IoT applications. Standard architectures, such as, rolling, unrolling and combinational were examined. S-box, which forms the core of AES was designed using composite field arithmetic and an optimized form was used in each architecture design to improve hardware efficiency. The design, verification and RTL synthesis of the algorithm was done using Xilinx Vivado 2018.3 simulator. Stringent area and power requirements being the prior criteria for IoT devices, the rolled architecture turned out to be the favorite candidate upon analysis of the result.

A. R. Chowdhury et al.,[2] Recently IoT devices are dominating the world by providing it's versatile functionality and real-time data communication. Apart from versatile functionality of IoT devices, they are very low-battery powered, small and sophisticated, and experience lots of challenges due to unsafe communication medium. It is present MAES, a lightweight version of Advanced Encryption Standard (AES) which meets the demand. A new 1-dimensional

Substitution Box is proposed by formulating a novel equation for constructing a square matrix in affine transformation phase of MAES. Efficiency rate of MAES is around 18.35% in terms of packet transmission which indicates MAES consumes less energy than AES and it is applicable for Resource Constraint Environments.

M. Xie et al.,[3] In this work, author propose a fast and efficient AES in-memory (AIM) implementation, to encrypt the whole/part of the memory only when it is necessary. Rather than adding extra processing elements to the cost-sensitive memory, we take advantage of NVM's intrinsic logic operation capability to implement the AES algorithm. We leverage the benefits (large internal bandwidth and dramatic data movement reduction) offered by the in-memory computing architecture to address the challenges of the bandwidth intensive encryption application. Embracing the massive parallelism inside the memory, AIM outperforms existing mechanisms with higher throughput yet lower energy consumption.

D. Bui et al.,[4] In this work, it is present propsoed hardware optimization strategies for AES for high-speed ultralow-power ultralow-energy IoT applications with multiple levels of security. Our design supports multiple security levels through different key sizes, power and energy optimization for both data path and key expansion. The estimated power results show that our implementation may achieve an energy per bit comparable with the lightweight standardized algorithm PRESENT of less than 1 pJ/b at 10 MHz at 0.6 V with throughput of 28 Mb/s in ST FDSOI 28-nm technology.

S. Chen et al.,[5] This work presents a very large-scale integration (VLSI) circuit design of a micro control unit (MCU) for wireless body sensor networks (WBSNs) in cost-intention. The proposed MCU design consists of an asynchronous interface, a multisensor controller, a register bank, a hardware-shared filter, a lossless compressor, an encryption encoder, an error correct coding (ECC) circuit, a universal asynchronous receiver/transmitter interface, a power management, and a QRS complex detector. A hardware-sharing technique was added to reduce the silicon area of a hardware-shared filter and provided functions in terms of high-pass, low-pass, and band-pass filters according to the uses of various body signals.

A. Jabbar et al.,[6] presents security architecture is designed that secures the data using encryption/decryption algorithm where the proposed algorithm is a hybrid encryption algorithm that uses the concept of EC-RSA, AES algorithm and Blowfish algorithm along with SHA-256 for auditing purpose. Presented experiment results show that the proposed concept is reasonable, it enhancing efficiency about 40% in terms of execution time i.e. encryption as well as decryption time and security and providing confidentiality of cloud data at could end.

Q. Wu et al.,[7] Broadcast encryption (BE) schemes allow a sender to securely broadcast to any subset of members but require a trusted party to distribute decryption keys. Group key agreement (GKA) protocols enable a group of members to negotiate a common encryption key via open networks so that only the group members can decrypt the cipher texts encrypted under the shared encryption key, but a sender cannot exclude any particular member from decrypting the cipher texts. In this work, we bridge these two notions with a hybrid primitive referred to as contributory broadcast encryption (ConBE).

A. Moradi et al.,[8] In this work. The attack is based on an also recently published correlation collision attack, which avoids the need for a hypothetical timing model for the underlying combinational circuit to recover the secret materials. The target platforms of our proposed attack are 14 AES ASIC cores of the SASEBO LSI chips in three different process technologies, 13 nm, 90 nm, and 65 nm. Successfully breaking all cores including the DPA-protected and fault attack protected cores indicates the strength of the attack.

B. Liu et al.,[9] By exploring different granularities of data-level and task-level parallelism, we map 16 implementations of an Advanced Encryption Standard (AES) cipher with both online and offline key expansion on a fine-grained many-core system. The smallest design utilizes only six cores for offline key expansion and eight cores for online key expansion, while the largest requires 107 and 137 cores, respectively. In comparison with published AES cipher implementations on general purpose processors, our design has 3.5-15.6 times higher throughput per unit of chip area and 8.2-18.1 times higher energy efficiency. Moreover, the design shows 2.0 times higher throughput than the TI DSP C6201, and 3.3 times higher throughput.

M. M. Wong et al.,[10] This work derive three novel composite field arithmetic (CFA) Advanced Encryption Standard (AES) S-boxes of the field GF(((22)2)2). The best construction is selected after a sequence of algorithmic and architectural optimization processes. Furthermore, for each composite field constructions, there exists eight possible isomorphic mappings. Therefore, after the exploitation of a new common subexpression elimination algorithm, the isomorphic mapping that results in the minimal implementation area cost is chosen. High throughput hardware implementations of our proposed CFA AES S-boxes are reported towards the end of this work.

Table 1: Summary of literature survey

Sr No.	Author Name	Publish Year	Proposed Work	Outcome
1	T. B. Singha	IEEE 2020	Advanced Encryption Standard for IOT	Improved area and power requirement
2	A. R. Chowdhury	IEEE 2018	Modified Advanced Encryption Standard	Efficiency is 18.35%
3	M. Xie	IEEE 2018	Advanced Encryption Standard	Encryption process by 80× for a 1-GB NVM
4	D. Bui	IEEE 2017	Block ciphers as advanced encryption standard	Proposed data path, 32-b key out of 128 b
5	Q. Wu	IEEE 2016	Broadcast encryption	Contributory broadcast Encryption
6	A. Moradi	IEEE 2013	14 AES ASIC cores	DPA-protected and fault attack
7	M. M. Wong	IEEE 2012	CFA AES S-boxes	Throughput 3.49 Gbps on a Cyclone I

III. ADVANCE ENCRYPTION STANDARD CONSTRAINT

AES is the short form of Advanced Encryption Standard.
• It is FIPS approved cryptographic algorithm used to protect electronic data.
• It is symmetric block cipher which can encrypt and decrypt information.
• Encryption part converts data into cipher text form while decryption part converts cipher text into text form of data.
• AES algorithm used different keys 128/192/256 bits in order to encrypt and decrypt data in blocks of 128 bits.
• AES is implemented in both hardware and software to protect digital information in various forms data, voice, video etc. from attacks or eavesdropping.
AES is slower than symmetric encryption. Therefore it is in general just used to encrypt a symmetric key that is used to encrypt the rest of the message. The main disadvantage of using a shared key in encryption is that you cannot use it to ensure non-repudiation. Every block is always encrypted in the same way.

- Hard to implement with software.
- AES in counter mode is complex to implement in software taking both performance and security into considerations.

Table 2: Comparison of different security algorithm

Sr No.	Parameter	Privacy Preserving	ID Cryptography	Ad-Dissemination	Token	Frame-Work
1	Complexity	Less	High	Average	Very less	High
2	Buffer Size	Less	More	Average	Very High	Average
3	Through put	High	Average	Average	Very less	High
4	Cost	High	Very less	Medium	Less	Less
5	Time	Medium	Less	Medium	Very High	Very less

6	Range	10 km	1-2 km	5 km	10 km	1-2 km

IV. CONCLUSION

This paper presents the literature survey and study of security algorithms for high speed and internet of things application and also introduced briefly the main ideas of IoT and called attention to the significance of having a protected structure for this new encouraging innovation. We went over the present difficulties related with giving protection which is the best basic segment, on the grounds that without enough security. Secondly different security techniques discussed and compare their performance. Also discuss existing AES algorithm studied and analysed well to promote the performance of the encryption methods also to ensure the security proceedings. Therefore AES has many advantages but if it will use IOT application then give more delay and consume large area and more power. In future it can be modified and design MAES sothat requirement of security in IOT application can be fulfil.

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